with the first pad and the second pad;

(b) the semiconductor chip has a third pad positioned adjacent to the second pad but away from the first pad on the circuit board; and

(c) the second pad on the circuit board and the third pad on the semiconductor chip are electrically connected through a bonding wire, so that the third pad on the semiconductor chip is electrically connected with the first pad on the circuit board through the bonding wire, the second pad on the circuit board, and the wire on the circuit board.

11. A semiconductor device, comprising:

a first semiconductor chip; and

a second semiconductor chip positioned on the first semiconductor chip; wherein

(a) the first semiconductor chip has a first pad, a second pad spaced away from the first pad in a direction along an outer peripheral edge of the second semiconductor chip, and a wire connecting between the first pad and the second pad on a surface of the first semiconductor chip supporting the second semiconductor chip, the wire being printed on the first semiconductor chip together with the first pad and the second pad;

(b) the second semiconductor chip has a third pad positioned adjacent to the second pad but away from the first pad on the first semiconductor chip; and

(c) the second pad on the first semiconductor chip and the third pad on the second semiconductor chip are electrically connected through a bonding wire, so that the

third pad on the second semiconductor chip is electrically connected with the first pad on the first semiconductor chip through the bonding wire, the second pad on the first semiconductor chip, and the wire on the first semiconductor chip.

12. A semiconductor device, comprising:

a first semiconductor chip;

a second semiconductor chip positioned on the first semiconductor chip; wherein

(a) the first semiconductor chip has a first pad, a second pad spaced away from the first pad in a direction along an outer peripheral edge of the second semiconductor chip, and a wire connecting between the first pad and the second pad on the first semiconductor chip, the first pad of the first semiconductor chip being positioned in its region facing to the second semiconductor chip while the second pad being positioned outside the region;

(b) the second semiconductor chip has a third pad corresponding to the first pad on the first semiconductor chip in its region facing to the first semiconductor chip so that the third pad of the second semiconductor chip faces the first pad of the first semiconductor chip; and

(c) the first pad on the first semiconductor chip and the third pad on the second semiconductor chip are electrically connected through a conductive member positioned between the first pad on the first semiconductor chip and the third pad on the second semiconductor chip.